UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,456	12/04/2001	Michael Kagan	3891-0101P	9182

44696 7590 05/28/2009

DR. MARK M. FRIEDMAN
C/O BILL POLKINGHORN - DISCOVERY DISPATCH
9003 FLORIN WAY
UPPER MARLBORO, MD 20772

EXAMINER	
DIVECHA, KAMAL B	

ART UNIT	PAPER NUMBER
2451	

NOTIFICATION DATE	DELIVERY MODE
05/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mark_f@friedpat.com
friedpat@yahoo.com
sharon_l@friedpat.com

Office Action Summary	Application No.	Applicant(s)	
	10/000,456	KAGAN ET AL.	
	Examiner	Art Unit	
	KAMAL B. DIVECHA	2451	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,11,12,14,16-19,31,34-39,41,42,44,46-49 and 64-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-9, 11-12, 14, 16-19, 31, 34-39, 41-42, 44, 46-49, 64-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Action is in response to communications filed 3/18/09.

Claims 1, 4-9, 11-12, 14, 16-19, 31, 34-39, 41-42, 44, 46-49, 64-66 are pending.

Claims 2-3, 10, 13, 15, 32-33, 40, 43, 45 and 60-63 were cancelled previously.

Claims 20-30 and 50-59 were withdrawn previously.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), **was filed on 3/18/2009** in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed **on 3/18/2009 has been entered.**

Response to Arguments

Applicant's arguments filed in the submission above have been fully considered **but they are not persuasive.**

In the submission, applicant argues in substance that:

a. Examiner has failed to make a prima facie case for obviousness of claim 1 and 31 because the proposed combination of the teachings of Pettey et al. and Gasbarro would be inoperative (remarks, pg. 22: second paragraph).

In response to argument [a], Examiner respectfully disagrees.

In the remarks, applicant asserts:

"Essentially, the Examiner has proposed using the SGL of Pettey et al. '712 as a WQE of Gasbarro et al. '004. But SGL 900 of Pettey et al. '712, as illustrated in Figure 9 of Pettey et al. '712 and as described in column 12 lines 24-36 of Pettey et aI., **is only "a portion of the WQE 800"** (Pettey et al. '712 column 12 line 26) and, as such, lacks essential information, such as destination QP 804 of WQE 800 as illustrated in Figure 8 of Pettey et al. '712, that would be needed by Gasbarro et al. '004 if SGL 900 of Pettey et al. '712 were to be used by Gasbarro et al. '004 in the rammer proposed by the Examiner. As stated in Gasbarro et al '004 column 7 lines 37-39 and column 17 lines 52-54 with regard to WQEs,

Such "WQEs" typically provide all the information needed to complete Send Queue mad Receive Queue operations. (emphasis added)

In the previous office action, applicant asserted that:

- Neither Pettey nor Gasbarro hinted or suggested anything resembling the response descriptors recited in claim 1 and 31 and/or Pettey handle...without creating and responding to a WQE or anything resembling a WQE, See: Final Rejection, pg. 2-3.

Now, applicant asserts that the combination is inoperative because Pettey uses SGL, a portion of WQE and **Gasbarro uses WQEs.**

Independent claim 1 recites:

A network interface adapter, comprising:

a host interface, for coupling to a host processor;

an outgoing packet generator, adapted to generate an outgoing request packet for delivery to a remote responder responsive to a request submitted by the host processor via the host interface;

a network output port, coupled to receive the request packet from the outgoing packet generator, so as to transmit the outgoing request packet over a network to the remote responder;

a network input port, for coupling to the network so as to receive an incoming response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester; and

an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate, in addition to the outgoing request packet, an outgoing response packet for transmission via the network output port to the remote requester;

wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface;

wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet;

wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface;

> wherein the incoming packet processor **is adapted to write a response descriptor** to a first memory location, in a memory separate from the network interface adapter, indicating the data to be read from the system memory responsive to the incoming read request packet;
>
> wherein the outgoing packet processor is **adapted to read the response descriptor** from the first memory location and, responsive thereto, to read the indicated data and to generate the outgoing response packet containing the indicated data;
>
> wherein the outgoing packet generator comprises a gather engine, which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets; and
>
> wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a second memory location, and wherein the gather engine is adapted to read information from the response descriptor and from the request descriptor and to gather the read data and the write data responsive thereto.

First, it should be noted that "during patent examination, the pending claims must be "given >their< broadest reasonable interpretation consistent with the specification." > In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)."

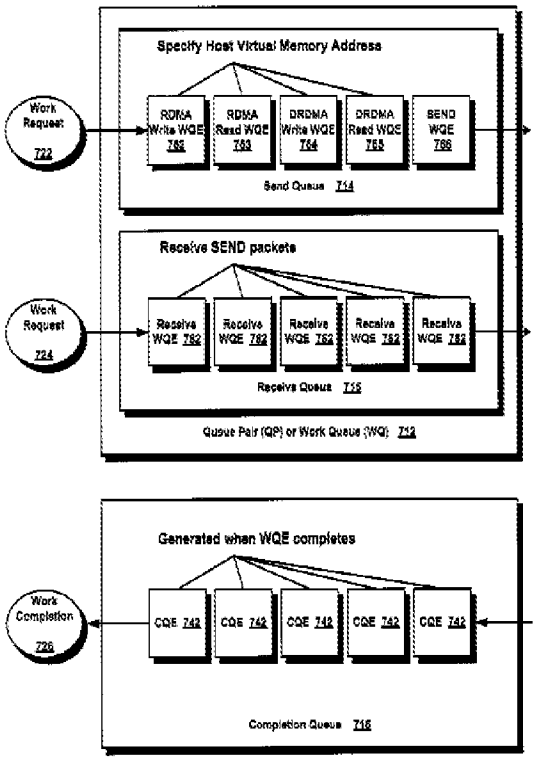
In this case, the independent claim 1 merely recites "response descriptors" indicating data to be read or write.

Secondly, it appears that applicant is misinterpreting the prima facie case of obviousness.

Pettey et al. (The Primary Reference)

Pettey explicitly discloses the usage of WQEs as follows:

FIG. 7b



Work Queue and Completion Queue Operation

Referring now to FIG. 7b, a block diagram illustrating in more detail a QP 712 of FIG. 7a and a Completion Queue 718 is shown. QP 712 is also referred to as a Work Queue 712. When the CPU 208 of FIG. 2 desires to send the host 102 a message, it submits a work request 722 to the TCA 202 Send Queue 714. The TCA 202 creates a Work Queue Entry (WQE) and places the WQE on the Send Queue 714. Among the WQE types are RDMA Write WQE 762, RDMA Read WQE 763, DRDMA Write WQE 764, DRDMA Read WQE 765, and SEND WQE 766.

The RDMA Write WQE 762, RDMA Read WQE 763, DRDMA Write WQE 764 and DRDMA Read WQE 765 specify, among other things, a virtual address in host 102 memory 124 for data transfers with the I/O unit 108. As the TCA 202 processes the Send Queue 714 WQEs, the TCA 202 generates one or more IB packets for each WQE and transmits the packets to the host 102. Additionally, the TCA 202 may receive in response one or more IB packets from the host 102 in the process of satisfying the WQE.

The Receive Queue 716 includes Receive WQEs 782. Receive WQEs 782 are placed on the Receive Queue 716 when the CPU 208 submits a work request 724 to the TCA 202. Receive WQEs 782 include address fields that point to buffers in the I/O unit 108 local memory 218 of FIG. 2 for receiving the payloads of SEND packets sent by the host 102, among other things.

The WQEs in the WQs 712 of FIGS. 7a and 7b may be associated with IB packets received from or destined for multiple of the IB hosts 102. Furthermore, WQEs in the WQs 712 may be associated with multiple IB packets received from or destined for the same IB host 102. Additionally, the WQEs in the WQs 712 of FIGS. 7a and 7b may include virtual addresses, discussed below with respect to FIGS. 8 and 10 through 13, which overlap with respect to the virtual address space of the IB hosts 102.

Stated another way, Pettey explicitly discloses posting the work request in form of WQEs to the respective queues. WQEs includes, among other things, the scatter/gather list, i.e. list of descriptors, indicating data to be read or write, e.g. col. 11 L59 to col. 12 L36.

However, Pettey does not explicitly disclose a gather engine for gathering both the write data and the read data from the system memory for inclusion in the respective outgoing packets, i.e. a single module or engine that gathers both the write data and read data.

Gasbarro et al. (The Secondary Reference)

Gasbarro explicitly discloses a shared module, i.e. **a micro engine that is capable of processing both types of WQEs, i.e. read WQEs and write WQEs through descriptor fetches**, e.g. col. 13 L37 to col. 14 L28.

As such, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro in order to gather both the read data and write data through a shared module.

Applicant should also note that SGLs are part of WQEs in both Pettey and Gasbarro. These SGLs are actual list of descriptors to be read in order to gather the outgoing data.

Merely changing the hardware structure from multiple structures or modules to a single shared structure or module does not make the combination inoperative.

For the at least these reasons, it is believed that the applicant have misinterpreted the prima facie of obviousness.

b. Applicant maintains the validity of the arguments in defense of claims 65 and 66 that were presented in the response, filed July 15, 2008…Applicant does not repeat those arguments, but merely points to the fact that Gasbarro teach specifically against the use of WQEs in responding to RDMA read request packets (remarks, pg. 23).

In response to argument [b], Examiner respectfully disagrees.

The response as presented in the previous office action is reproduced herein.

Gasbarro discloses (col. 12 L32 to col. 13 L36):

FIG. **6** illustrates an example host system using NGIO/InfiniBand™ and VI architectures to support data transfers via a switched fabric **100'**. As shown in FIG. **6**, the host system **130** may include, in addition to one or more processors **202** containing an operating system (OS) stack **500**, a host memory **206**, and at least one host-fabric adapter (HCA) **120** as shown in FIGS. **2**, **4A–4B** and **5**, a transport engine **600** provided in the host-fabric adapter (HCA) **120** in accordance with NGIO/InfiniBand™ and VI architectures for data transfers via a switched fabric **100'**. One or more host-fabric adapters (HCAs) **120** may be advantageously utilized to expand the number of ports available for redundancy and multiple switched fabrics.

As shown in FIG. **6**, the transport engine **600** may contain a plurality of work queues (WQ) formed in pairs including a Receive Queue ("RQ" for inbound requests) and a Send Queue ("SQ" for outbound requests), such as work queue pairs (WQP) **610A–610N** in which work requests "WQEs" may be posted to describe data movement operation and location of data to be moved for processing and/or transportation via a switched fabric **100'**, and completion queues (CQ) **620** may be used for the notification of work request completions. Alternatively, such a transport engine **600** may be hardware memory components of a host memory **206** which resides separately from the host-fabric adapter (HCA) **120** so as to process completions from multiple host-fabric adapters (HCAs) **120**, or may be provided as part of kernel-level device drivers of a host operating system (OS). All work queues (WQs) may share physical ports into a switched fabric **100'** via one or more host-fabric adapters (HCAs) **120**.

Each work queue pair (WQP) can be programmed with various sized WQEs. Each WQE may be accessed to obtain control data supplied within. One of the control fields in the WQE may be a Data Segment. Data Segments are scatter

gather lists pointing to memory regions of system memory **206** where message data is to be transmitted from or where incoming message data is to be written thereto. WQEs can contain various amounts of Data Segments as long as the total does not exceed the programmed size of the WQE.

The Send Queue ("SQ" for outbound requests) of the work queue pair (WQP) may be used to as an "initiator" which requests, for example, normal message sends to remote VIs, remote direct memory access "RDMA" reads which request messages to be read from specific memory locations of a target system, via a switched fabric **100'**, and remote direct memory access "RDMA" writes which request messages to be written onto specific memory locations of a target system, via a switched fabric **100'**, as described with reference to FIGS. **3A–3D**.

The Receive Queue ("RQ" for inbound requests) of the work queue pair (WQP) may be used as a "responder" which receives requests for messages from normal sends, RDMA reads and RDMA writes from a target system, via a switched fabric **100'**, as described with reference to FIGS. **3A–3D**.

In such an example data network, NGIO/InfiniBand™ and VI hardware and software may be used to support data transfers between two memory regions, often on different systems, via a switched fabric **100'**. Each host system may serve as a source (initiator) system which initiates a message data transfer (message send operation) or a target system of a message passing operation (message receive operation). Examples of such a host system include host servers providing a variety of applications or services and I/O units providing storage oriented and network oriented IO services. Work requests in the form of "WQEs" (data movement operations such as message send/receive operations and RDMA read/write operations) may be posted to work queue pairs (WQPs) **610A–610N** associated with a given fabric adapter (HCA), one or more channels may be created and effectively managed so that requested operations can be performed.

In other words, **the receive queue is used as responder which receives requests for messages from normal sends, RDMA reads, i.e. incoming RDMA requests** and RDMA writes from a target system.

Work requests in form of WQEs (data movement operations such as message send/receive operations and **RDMA read/write operations) are posted to work queue pairs associated with a given fabric adapter HCA, whether it be incoming or outgoing work requests.**

Furthermore, **WQEs uses data segments which are scatter gather lists pointing to memory regions of system memory where message data <u>is to be transmitted from, i.e. uses posted WQEs to convey from where to transmit the data,</u>** or where incoming message data is to be written thereto.

As such, it's clearly seen that Gasbarro posts WQEs in response to both the incoming and outgoing requests, acting both as the requestor and responder, by utilizing the WQEs.

Furthermore, applicant asserts that "Applicant does not repeat…for example in column 7 lines 46-49: For an RDMA operation…".

This example and/or assertion is presented for the first time in this application.

In any event, the cited portion by the applicant in fact clearly shows and actually encourages the usage of WQEs for the RDMA operation as evidenced herein.

Work requests submitted by a consumer in a form Work Queue Elements "WQEs" are posted onto appropriate work queues (WQs) from the host system **130** to describe data movement operation and location of data to be moved for processing and/or transportation, via the switched fabric **100**. Such "WQEs" typically provide all the information needed to complete Send Queue and Receive Queue operations.

There may be several classes of Send Queue operations, including Send, Remote Memory Access (RDMA), and Memory Binding. For a Send operation, the WQE specifies a block of data in the consumer's memory space for the hardware to send to the destination, letting a receive WQE already queued at the destination specify where to place that data. For an RDMA operation, the WQE also specifies the address in the remote consumer's memory. Thus an RDMA operation does not need to involve the receive work queue of the destination.

The section shows that "**for the RDMA operation**, **the WQE specifies** the address in the remote consumer's memory". It's unclear how the process **of not involving** the receive work queue of the destination, i.e. where the data packet is to be transferred, indicate against the use of WQEs when the passage above clearly encourages the usage of WQEs.

For the at least these reasons, the REJECTION IS MAINTAINED.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1, 4-9, 11-12, 14, 16-19, 31, 34-39, 41-42, 44, 46-49 and 64-66 are rejected under **35 U.S.C. 103(a)** as being obvious over Pettey et al. (hereinafter Pettey, U. S. Patent No. 6,594,712 B1) in view of Gasbarro et al. (hereinafter Gasbarro, U. S. Patent No. 6,948,004 B2).

As per claim 1, Pettey discloses a network interface adapter (fig. 3 item #202: Channel adapter), comprising:

a host interface for coupling to a host processor (fig. 3 item #214: interfaces for coupling);

an outgoing packet generator, adapted to generate an outgoing request packet for delivery to a remote responder responsive to a request submitted by the host processor via the host interface (col. 7 L65 to col. 8 L7, col. 14 L20-39, fig. 3 item #306: Bus router generates the packets);

a network output port, coupled to receive the request packet from the output packet generator, so as to transmit the outgoing request packet over a network to the remote responder (col. 9 L1-5, fig. 3 item #308: network interfaces);

a network input port, for coupling to the network so as to receive an incoming response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester (fig. 3 item #308: network interfaces and fig. 2 item #204);

an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate in addition to the outgoing request packet, an outgoing response packet for transmission via the network output port to the remote requester (col. 10 L4-9, col. 14 L40-54 and fig. 3 item #306: Bus router processes packets as well),

wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface (fig. 18a: describes the process of RDMA WRITE operation; fig. 16: shows the I/O WRITE operation, col. 11 L18-27, col. 13 L18-57),

wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet (fig. 18a, fig. 16, col. 13 L58 to col. 14 L9), and

wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface (fig. 15: describes an incoming read request packet, col. 11 L17-67, col. 13 L58 to col. 14 L9, L40-65 and col. 15 L65 to col. 16 L6);

wherein the incoming packet processor is adapted to write a response descriptor to a first memory location, in a memory separate from the network interface adapter, indicating the data to be read from the system memory responsive to the incoming read request packet (col. 14 L10-67, fig. 2 item #218, fig. 7B: the WQE are stored in local memory, separate from the TCA, and col. 25 L10-26);

wherein the outgoing packet processor is adapted to read the response descriptor from the first memory location and, responsive thereto, to read the indicated data and to generate outgoing response packet containing the indicated data (col. 9 L1-5, col. 11 L54 to col. 12 L67, col. 22 L39-67).

wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a second memory location (col. 11 L18 to col. 12 L45 and fig. 7b).

However, Pettey does not explicitly disclose the GATHER engine which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets and a process adapted to read information from the descriptors and

to gather the read data and the write data responsive thereto (i.e. Pettey does not explicitly disclose using a shared/single module or engine to gather both the write data and read data).

Gasbarro explicitly discloses an interface adapter (fig. 7) comprising a gather engine providing a gather list describing virtual addresses to fetch outgoing whether it's a read or write data from local system memory for inclusion in the outgoing packets (col. 13 L37 to col. 14 L28: MC subsystem including one micro engine, col. 15 L20-67, col. 21 L16-56: the gather engine implicitly gathers the data in response to either write or read request regardless of incoming and outgoing packets), a scatter/gather engine adapted to read information from the indicators or descriptors, i.e. WQEs and to gather or fetch the read data and the write data (col. 8 L28-41, col. 12 L32 to col. 13 L36).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro (hereinafter Pettey-Gasbarro) in order to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets.

One of ordinary skilled in the art would have been motivated because it would have enabled the process of fetching outgoing data from system memory [whether it's a read or write data] via one/single module or engine (Gasbarro: col. 8 L28-34, col. 13 L1-32).

As per claim 4, Pettey-Gasbarro discloses the interface adapter wherein the outgoing packet generator comprises a plurality of schedule queues (Pettey: fig. 7a block #108: Queue Pairs), and is adapted to generate the outgoing request packet (Pettey: fig. 16) and the outgoing response packet responsive to respective entries placed in the schedule queues of the plurality of

schedule queues (Pettey: col. 11 L18-53: WQEs are placed in the respective queue pairs, col. 14 L10-54, fig. 18a item #1808, 1822, fig. 22a item #2224, 2226 and fig. 15).

As per claim 5, Pettey-Gasbarro discloses the interface adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances (i.e. over queue pairs), and wherein the outgoing request packet and the outgoing response packet are associated with respective instances among the plurality of transport service instances (Pettey: fig. 7a item #108: send/receive queues), and wherein the outgoing packet generator is adapted to assign the transport service instances of the plurality of transport service instances to the schedule queues of the plurality of schedule queues based on service parameters of the instances (Pettey: col. 11 L1-21: plurality of QPs exist and/or are configured/assigned based on send/receive functions), and to place the entries in the schedule queues corresponding to the transport service instances with which the incoming and outgoing packets are associated (Pettey: col. 8 L2-26, col. 11 L1-36: placing WQEs and col. 14 L10-54).

As per claim 6, Pettey-Gasbarro discloses the adapter of claim 5, wherein the outgoing packet generator comprises one or more execution engines, which are adapted to generate the outgoing request packet and the outgoing response packet responsive to a list of work items respectively associated with each of the transport service instances (Pettey: col. 11 L18-53, col. 14 L10-54) and assigning the transport service instances of the plurality of transport service instances to the one or more execution engines for execution of the work items (Pettey: col. 11 L1-21: plurality of QPs exist and/or are configured/assigned based on send/receive functions).

However, Pettey does not disclose a scheduler, which is coupled to select the entries from the plurality of schedule queues.

Gasbarro discloses an adapter comprising a scheduler for scheduling the next virtual interface to the context manager and supporting priority of traffic for data packets associated with send queue and receive queue of the work queue pair, i.e. selecting the work items based on priority (col. 15 L50-58).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view Gasbarro, in order to include a scheduler for selecting the entries from the queues and to assign the instances to the execution engines for execution of the work items responsive to the service parameters.

One of ordinary skilled in the art would have been motivated because a scheduler would have supported the priority of traffic for data packets associated with send queue and receive queue of the work queue pair (Gasbarro, col. 15 L50-55).

As per claim 7, Pettey-Gasbarro discloses an adapter wherein the transport service instances comprise queue pairs (Pettey: col. 11 L1-50; Gasbarro: fig. 7a-7b: shows plurality of queues including queue pairs).

As per claim 8, Pettey-Gasbarro discloses the adapter of claim 4, wherein the outgoing packet generator comprises one or more control registers to which the host processor and incoming packet processor write in order to place the entries in the queues (Pettey: col. 17 L20-56).

However, Pettey does not explicitly disclose the one or more register to be a doorbell registers.

Gasbarro explicitly discloses a channel adapter comprising one or more doorbell registers (col. 15 L20-50).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to replace the one or more control registers with the doorbell registers, since Gasbarro teaches and discloses the usage of doorbell registers.

One of ordinary skilled in the art would have been motivated because doorbell registers allows software the capability to enable automatic event generation, and making doorbell registers memory mapped allows applications the ability to write those registers thereby controlling event generation (Gasbarro: col. 15 L20-32).

As per claim 9, Pettey-Gasbarro discloses an adapter wherein the incoming request packet comprises a write request packet carried over the network on a reliable transport service, and wherein responsive to the incoming write request packet, the incoming packet processor is adapted to add an entry to the entries placed in the queues, such that responsive to the entry, the outgoing packet generator generates an acknowledgement packet (Pettey: col. 11 L1-58; Gasbarro: col. 19 L55 to col. 20 L33).

As per claim 11, Pettey-Gasbarro discloses the adaptor of claim 1, including the process of receiving a read request (fig. 15 item #1000); the process of receiving a write request (fig. 16 item #1000); and the process of conveying or sending the write data to the host interface (fig. 15 item #1100).

However, Pettey does not disclose the process of receiving an incoming write request packet containing write data to be written to a system memory accessible via the host interface

after receiving the incoming read request packet, and the process of conveying the write data to the host interface without waiting for execution of the response descriptor.

Gasbarro discloses the adaptor which supports the priority of traffic for data packets associated with send Queue and Receive Queue of the work queue pair, i.e. selecting the work items for processing based on priority (col. 15 L50-58; See also applicant specification, pg. 26: inherent IB convention).

Therefore, it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey (i.e. modify Pettey's figure 15 and 16 so that the incoming packet processor of the adapter (see the rejected claim 1) is configured so that the write request work queue entry is executed first based on priority with respect to read response work queue entry or response descriptor) in order to convey the write data to the host interface without waiting for execution of the read response work item.

One of ordinary skilled in the art would have been motivated because it would enable processing the prioritized packets (Gasbarro: col. 15 L50-58).

As per claim 12, Pettey-Gasbarro discloses an adapter wherein the incoming packet processor is configured so that when it receives an incoming write request packet containing write data to be written to a system memory accessible via the host interface before receiving the incoming read request packet, it prevents execution of the read response work item or response descriptor until the write data have been written to the system memory (Pettey: col. 21 L12 to col. 22 L6; Gasbarro: col. 15 L50-58: based on priority).

As per claim 14, Pettey-Gasbarro discloses an adapter wherein the outgoing packet generator is adapted, upon generating the outgoing request packet, to notify the incoming packet

processor to await the incoming response packet so as to write a completion message to the host interface when the awaited packet is received (Pettey: col. 20 L17-32).

As per claim 16, Pettey-Gasbarro discloses an adapter wherein the incoming read request packet is **one of a** plurality of incoming read request packets, and wherein the incoming packet processor is adapted to write a list of corresponding response descriptor to the first memory location each said response descriptor indicating the data to be read from the system memory responsive to the corresponding incoming read request packet, responsive to which the outgoing packet processor is adapted to generate the outgoing response packet as part of a sequence of such packets (Pettey: fig. 19a, fig. 20 and fig. 9; col. 23 L20 to col. 24 L27; col. 11 L18-37, fig. 7b, fig. 2 and col. 14 L10-20).

As per claim 17, Pettey-Gasbarro discloses an adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the incoming packet processor is adapted to prepare the list of the response descriptors for each of the instances as a part of a response database held for the plurality of the instances in common (Gasbarro: fig. 3 item #308, fig. 19b item #508, and fig. 23).

As per claim 18, Pettey-Gasbarro discloses an adapter wherein the transport service instances comprise queue pairs (Pettey: col. 11 L1-17; Gasbarro: fig 7a item #712).

As per claim 19, Pettey-Gasbarro discloses the adapter wherein the request comprises a write request, which is submitted by the host processor by generating a request descriptor indicating further data to be read from the system memory for inclusion in the outgoing packet (fig. 10), and wherein the output packet generator is adapted to read the request descriptor and,

responsive thereto, to generate the outgoing request packet as a write request packet containing the indicated further data (Pettey: fig. 18a item #1832; col. 12 L58 to col. 13 L18, col. 15 L17-31 and fig. 16).

As per claim 64, Pettey-Gasbarro discloses an adapter wherein the memory separate from the network interface is the system memory (Pettey: fig. 2 item #218).

As per claim 65, Pettey-Gasbarro discloses the adapter wherein the incoming read request packet is a RDMA read request packet and wherein the response descriptor is a quasi-WQE (i.e. work item; Pettey: fig. 7b, col. 11 L1-53; Gasbarro: col. 7 L33-67, col. 13 L15 to col. 14 L28).

As per claims 31, 34-39, 41-42, 44, 46-49 and 66, they do not teach or further define over the limitations in claims 1, 4-9, 11-12, 14, 16-19 and 64-65. Therefore claims 31, 34-39, 41-42, 44, 46-49 and 66 are rejected for the same reasons as set forth in claims 1, 4-9, 11-12, 14, 16-19 and 64-65.

Additional References

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Beukema et al., U. S. Patent No. 6,578,122 B2: Using an Access Key to protect and point to regions in windows for infiniband.

b. Avery, U. S. Patent No. 6,611,883 B1: Method and Apparatus for Implementing PCI DMA speculative prefetching in a message passing queue oriented bus system.

c. Thomas et al., U. S. Patent No. 5,922,046: Method and Apparatus for avoiding control reads in a network node.

d. Coffman et al., U. S. Patent No. 6,718,370 B1: Completion Queue management mechanism.

e. Pettey, US 7,149,817: Infiniband TM Work Queue to TCP/IP translation.

Conclusion

The teachings of the prior art should not be restricted and/or limited to the citations by columns and line numbers, as specified in the rejection. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in its entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

In the case of amendments, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and support, for ascertaining the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMAL B. DIVECHA whose telephone number is (571)272-5863. The examiner can normally be reached on Increased Flex Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KAMAL B DIVECHA/
Examiner, Art Unit 2451